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Interleaved High Step-Down Synchronous Converter

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ABSTRACT
For low output voltage, high output current systems applications, Synchronous switching power converters give better performance than non synchronous converters. This paper presents an interleaved synchronous buck converter which has low switch voltage stress with high conversion ratio. The input current can be shared among the inductors so that high reliability and efficiency can be obtained and ripples also reduced, the converter performance can be improved. Thus converter features automatic uniform current sharing characteristic of the interleaved phases without adding extra circuitry or complex control methods. Capacitors switching circuits are combined with interleaved four-phase buck converter for getting a high step-down conversion ratio without adopting an extreme short duty ratio. Synchronous rectifier technology is adopted to increase the converter efficiency. A 30V input voltage, 1.8V output voltage, circuit is simulated to verify the performance. The simulation is done in MATLAB/SIMULINK R2012a.

Keywords: *Buck Converter, Four phase, Interleaved, MATLAB/SIMULINK, Synchronous*

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I. INTRODUCTION

Interleaving technique connects converter-converter in parallel to share the power flow between two or more conversion chains [1]. It gives a reduction in the size, weight and volume of the inductors and capacitors. A proper control of the parallel converter will reduce the ripple amount at the input and output of the power conversion system, which leads to a significant reduction of current and voltage ripples. Interleaving technique is used in some applications due to its advantages regarding filter reduction, dynamic response and power management. Interleaved Buck DC-DC converters have presently acquired a wide importance owing to their application in voltage regulator modules. Interleaved Buck Converter (IBC) is adopted as a good solution for low voltage and high current applications [5]. Investigation of interleaving technique for step down topology mainly points out the benefits interleaving offers to future microprocessors. Synchronous switching power converters give better performance than non-synchronous converters in low output voltage, high output current systems applications [6]. This paper presents an interleaved synchronous buck converter which has low switch voltage stress with high conversion ratio.

II. INTERLEAVED HIGH STEP-DOWN SYNCHRONOUS RECTIFIER

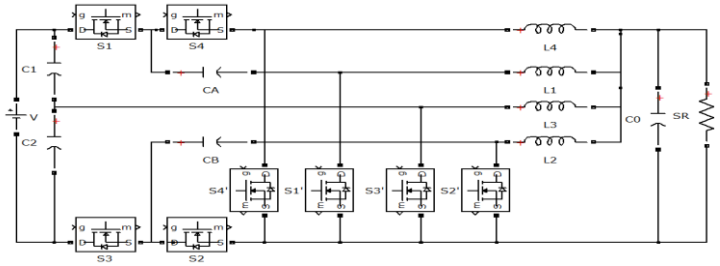

Fig. 1. Synchronous interleaved buck converter

Synchronous Buck converter is like to the preceding conventional buck converter, excluding the diode is connected in parallel with a new transistor. The knowledge of a synchronous buck converter is to custom a MOSFET as a rectifier that has very short forward voltage drop as related to a normal rectifier. By dropping the diodes voltage drop, the overall productivity for the buck converter can be enhanced. The synchronous rectifier needs another PWM signal that is the counterpart of the main PWM signal. S1 is on once S01 is off and reverse is true. This pwm arrangement is called Complementary PWM. Power losses in the SBC are divided in three categories: load dependant conduction losses, frequency dependant switching losses and additional losses (including gate drive loss). The expression for conduction losses is the same for both, DCM and CCM. The

synchronous MOSFET conducts when the power switch turns off and provides a path for the inductor current. For the low side MOSFET, the on-resistance R_{DSON} is the primary parameter for selection. Because of the small duty cycle of the high side, the on-resistance determines the power dissipation in the low side MOSFET and therefore significantly affects the efficiency of the DC-DC converter. For high current applications, it may be necessary to use two MOSFETs in parallel for each phase. This effectively reduces the RDSON and therefore reduces the conduction losses. From the reference papers it is clear that synchronous rectifier has more efficiency than rectifier which uses diodes. Power losses in synchronous buck converter are mainly switching losses and losses due to internal resistance [6].

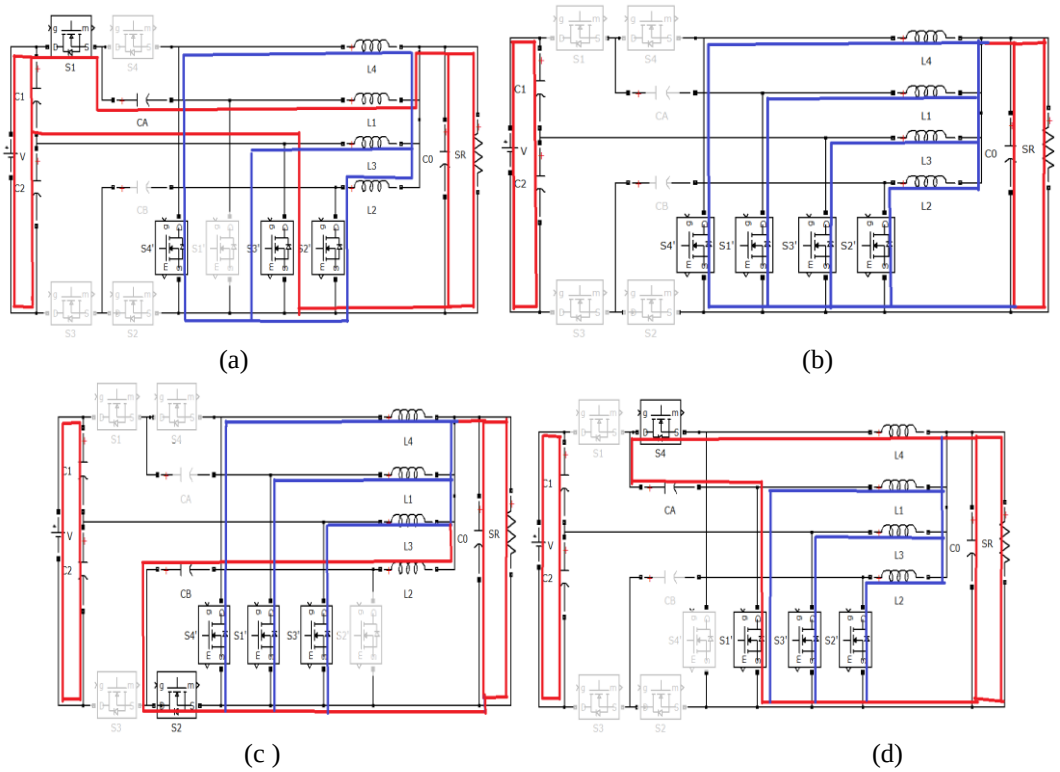

Fig.2. (a). Mode 1, (b) Mode 2,4,6,8, (c) Mode 3, (d) Mode 5

Mode 1: In this operation mode, switch S_1 is turned on, switch S_2, S_3 and S_4 remain on. Synchronous switch S_{01} are turned off and S_{02}, S_{03} and S_{04} remain on. The corresponding equivalent circuit is shown in figure 2(a). From figure 2(a) it is seen that the stored energy of C_1 is discharged to C_A, L_1, and output load and current i_{L2}, i_{L3} and i_{L4} are freewheeling through S_{02}, S_{03} and S_{04} respectively. The V_{L2}, V_{L3} and V_{L4} are equal to V_{C0}, and hence, i_{L2} , i_{L3} and i_{L4} decrease linearly. The voltage across S_{01} is clamped to V_{C1} - V_{CA}. The voltage across switch S_3 is clamped to - V_{CB} and the voltage across the switch S_2 and S_4 are clamped to V_{CB} and V_{C1} respectively.

Mode 2, 4, 6, 8: For this operation mode, switch S_1, S_2, S_3 and S_4 are off. The corresponding equivalent circuit is shown in figure2 (b), one can see that i_{L1} , i_{L2} , i_{L3} and i_{L4} are freewheeling through S_{01}, S_{02}, S_{03} and S_{04} respectively. All V_{L1}, V_{L2}, V_{L3} and V_{L4} are equal to -V_{C0}, and hence, i_{L1}, i_{L2}, i_{L3} and i_{L4} decrease linearly. During this mode, the voltage across S_1, namely V_{S1}, is equal to the difference of V_{C1} and V_{CA}, andV_{S2} is clamped at V_{CB}. Similarly, the voltage across S_3, namely V_{S3}, is equal to the difference of V_{C2} and V_{CB}, and V_{S4} is clamped at V_{CA}.

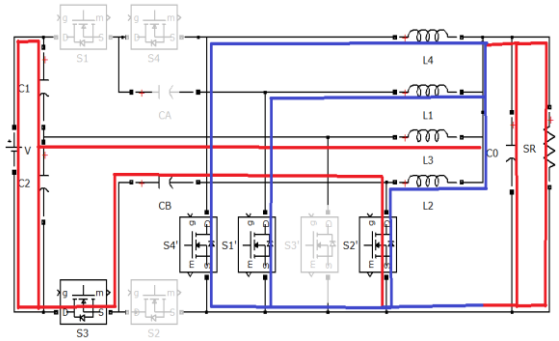

Fig. 3. Mode 7

Mode 3: During this mode, S_{02} becomes turned off while S_2 is turned on. Stored energy of C_B is discharged to L_2 and output load and i_{L1}, i_{L3} and i_{L4} are freewheeling through S_{01}, S_{03} and S_{04} respectively. The inductor L_1, L_3 and L_4 are releasing energy to output load. The voltage across diode S_{02} is clamped to V_{CB}. The voltage across switch S1 is clamped to V_{C1} - V_{CA} and the voltage across the switch S_3andS_4 are clamped to V_{C2} and V_{CA} respectively.

Mode 5: During this mode, S_{04} becomes turned off while S_4 is turned on. Stored energy of C_A is discharged to L_4 and output load and i_{L1}, i_{L2} and i_{L3} are freewheeling through S_{01} , S_{02} and S_{03} respectively. The inductor L_1, L_2 and L_3 are releasing energy to output load. The voltage across diodes S_{04} is clamped to V_{CA}. The voltage across switch S_1 is clamped to V_{C1} - V_{CA} and the voltage across the switch S_2 and S_3 are clamped to V_{CB} and V_{C2} - V_{CB} respectively.

Mode 7: During this mode, S_{03} becomes turned off while S_3 is turned on. Stored energy of C_2 is discharged to C_B, L_3, and output load and i_{L1} , i_{L2} and i_{L4} are freewheeling through S_{01} , S_{02} and S_{04} respectively. All V_{L1} , V_{L2} and V_{L4} are equal to $-V_{C0}$, and hence i_{L1} , i_{L2} and i_{L4} decrease linearly. The voltage across switch S_{03} is clamped to V_{C2} - V_{CB}. The voltage across switch S_1 is clamped to Vi_n - (V_{CA} + V_{CB}) and the voltage across the switch S_2 and S_4 are clamped to V_{CB} and V_{CA} respectively.

III. SIMULATION MODELS AND RESULTS

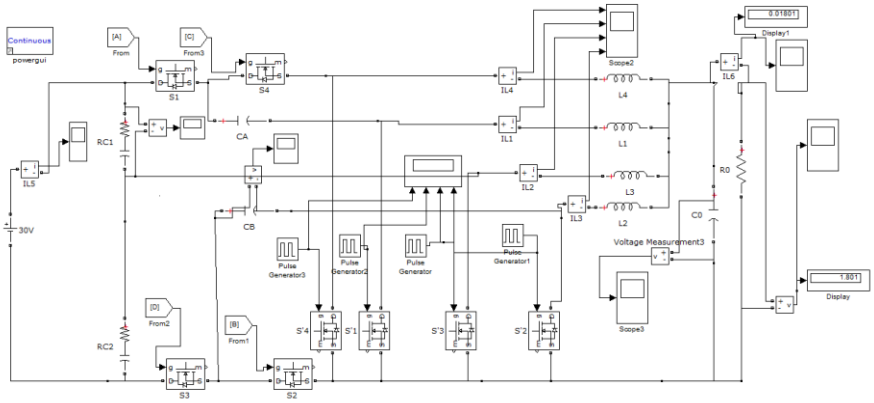

Fig. 4. Simulink Model of synchronous interleaved buck converter

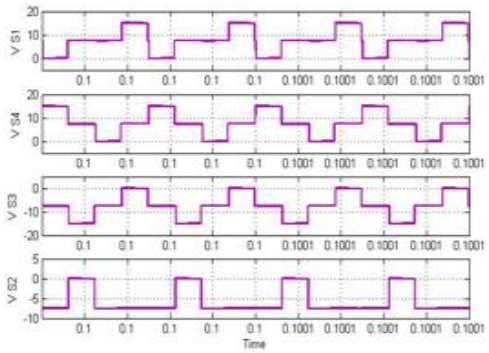

Fig. 5. Voltage Stress of main MOSFETs

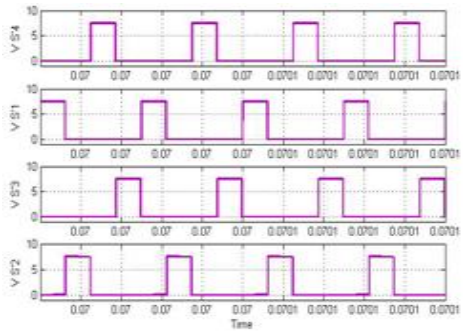

Fig. 6. Voltage across synchronous MOSFETs

Table 1: Comparative study between conventional and proposed buck converter

Stress	Conventional IBC	Proposed Converter
Conversion Ratio	D	D/4
Voltage Stress of Switch 1,3	V	V/2 for both
Voltage Stress of Switch 2,4	V	V/4 for S2 V/2 for S4
Voltage Stress of Diode	V	V/4
Automatic uniform current sharing	NO	YES

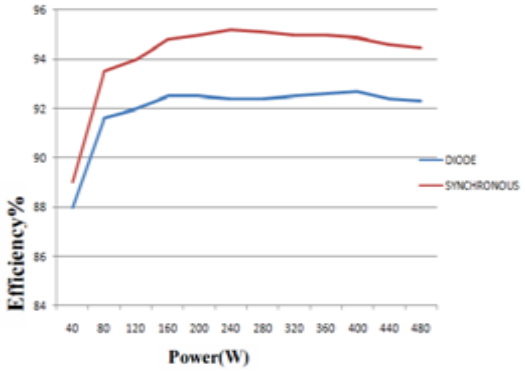

Fig. 6. Efficiency Vs power curve of proposed and conventional converter.

Simulation of interleaved high step down synchronous rectifier results a output voltage of 1.8 V for a input of 30 V. For demonstrating the performance of this converter, the transformer less interleaved four phase converter is compared with conventional IBC as shown in Table 1. Efficiency of Interleaved high step-down synchronous rectifier is 2% more than conventional interleaved converter.

IV. CONCLUSIONS

Interleaved High Step-down Synchronous Rectifier with high efficiency, low losses is introduced. Synchronous switching power converters give better performance than non-synchronous converters in low output voltage, high output current systems applications. This converter topology possesses the low switch voltage stress characteristic thereby, enables the use of low voltage rating MOSFETs to reduce both switching and conduction losses. It features automatic uniform current sharing and high step down conversion ratio. By analyzing results of simulation it is clear that it have very low output ripple. In the Interleaved High Step-down Synchronous Rectifier, synchronous technique is combined with interleaved four-phase buck converter in order to get a high step-down conversion ratio with high efficiency. This converter topology possesses the low switch voltage stress characteristic. Synchronous rectifiers are used, further reducing the conduction losses caused by the freewheeling diodes. Efficiency of interleaved high step-down synchronous rectifier is 2 to 3% more than conventional interleaved converter.

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